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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,238	06/24/2003	Rong Yin	02-C-086	5616

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EXAMINER	
CHANG, JOSEPH	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,238	YIN ET AL.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,9,14,15,17-19,22 and 25* is/are rejected.

7)☒ Claim(s) *3,6-8,10-13,16,20,21,23,24 and 26-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Startup Circuit and Method for Staring an Oscillator after Power-up.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-5, 9, 14-15, 17-19, 22 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al. (US 6670860).

Regarding Claim 1, Kobayashi et al. discloses in Figures 2 and 3 a circuit (10), comprising: an oscillator circuit (2) adapted to oscillate at predetermined frequency (intrinsic resonant frequency of piezoelectric oscillator 2); and an enable circuit (Starter Circuit 34 and Control Circuit 43) having an input (Reset S3) and an output (S2) coupled to the oscillator circuit (2 via Switch FET 31), the output of the enable circuit (S2) having an inactive state (Logic High-level, see Figure 3, (c), see Col.3, lines 57-65) upon the circuit being powered up (VDD1, Col 3, lines 59-60) and an active state (Logic Low-

level) enable the oscillator circuit oscillate a predetermined period of time (from t6 to t8, Col. 5, lines 12-21) following the input (S3, resets the counter) of the enable circuit transitioning from the inactive state (from Logic High-level just before t6, see figure 3(c)).

Regarding Claim 2, Kobayashi et al. discloses that the enable circuit (Starter Circuit 34 and Control Circuit 43) comprises a counter (42) having an enable input (S3) coupled to the input of the enable circuit and an output (S4) coupled to the output of the enable circuit (S2 via 32 and 33). It is noted that the recitation "coupled to" is a broad term that any points are "coupled to" in any given circuitry unless there is a modifier such as "directly coupled to".

Regarding Claim 4, Kobayashi et al. discloses that the counter (42) includes a control input (S3, triangle) which, when in an active state (t6-t8), places the counter in a predetermined state (t8), the control input (S3) being coupled to power-on-reset circuitry (44). It is noted that the control input of the counter is the same as the input of the enable circuit.

Regarding Claim 5, Kobayashi et al. discloses that the control input is reset input (S3) that selectively resets (when VDD2 is high) the counter.

Regarding Claim 9, Kobayashi et al. discloses a method for enabling an oscillator circuit to oscillate, comprising: receiving a power-on-reset signal (S3); generating an enable signal (S2) that transitions from an inactive state to an active state (transition at t6, see Figure 3) so as to enable the oscillator circuit to oscillate (logic low-level S2 turns switch 31 on to enable the oscillator 2), the enable signal transitions to the active state

(logic low-level) a period of time (t6-t8, Counter 42 starts counting after Reset signal S3 at t6) following the power-on-reset signal transitioning from a reset state (see Figure 3(e), a reset state right before t6); and applying the enable signal (S2) to the oscillator circuit (2).

Regarding Claim 14. Kobayashi et al. discloses a circuit (10), comprising: an oscillator circuit (piezoelectric oscillator 2) capable of oscillating at predetermined frequency (intrinsic resonant frequency of piezoelectric oscillator 2); and an enable circuit (Starter Circuit 34 and Control Circuit 43) having an output (S2) coupled to the crystal oscillator circuit (piezoelectric oscillator 2 via Switch FET 31), the output of the enable circuit transitioning (t6) from an inactive state (Logic High-level) to an active state (Logic Low-level) predetermined period of time (t6-t8, Col. 5, lines 12-21) following the circuit being initially powered (VDD1, Col 3, lines 59-60), for enabling the oscillating the oscillator circuit oscillate (S2 is logic low-level after t6).

Regarding Claim 15. Kobayashi et al. discloses that the enable circuit comprises a counter (42) having an output (S4) coupled to the output of the enable circuit (S2 via 32 and 33).

Regarding Claims 17-18, Kobayashi et al. discloses that the counter (42) includes is a control input (S3) which selectively places (when VDD2 is High) the counter in a predetermined state (S3 resets Counter 42 to start counting SP signals when VDD2 is High until it reaches a predetermined value, see Figure 3).

Regarding Claim 19, Reset Circuit 44 (power-on-reset circuit) produce reset signal S3 that is the control input of Counter 42. The reset signal is generated when VDD2 is high (power is on).

Regarding Claim 22, Kobayashi et al. discloses a power-on-reset circuit (Reset Circuit 44, the reset signal is generated whenever VDD2 is high (power is on)), wherein the enable circuit (Starter Circuit 34 and Control Circuit 43) comprises a counter (42) having an output (S4) coupled to the output of the enable circuit (S2 via 32 and 33) and a control input (S3) used to selectively place (when VDD2 is High) the counter in a known state (S3 resets Counter 42 to start counting SP signals when VDD2 is High until it reaches a predetermined value) the control input (S3) being coupled to the output of the power-on-reset circuit (44).

Regarding Claim 25, Kobayashi et al. discloses a system (10), comprising: a circuit (2); and oscillator circuitry (Starter Circuit 34) for receiving an enable signal (S4) and generating an oscillating signal (S1, see Figure 3) at an output of the oscillator circuitry (output of 33), the output of the oscillator circuitry being coupled to the circuit (2 via 31), the oscillating signal oscillating a predetermined period of time (RC time constant, 32) following the received enable signal (S4) transitioning to a first logic state (Logic High-level, see Figure 3 (g)).

Allowable Subject Matter

Claims 3, 6-8, 10-13, 16, 20-21, 23-24 and 26-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Kobayashi et al., taken alone or in combination of other references, does not teach or fairly suggest a ring oscillator (Claims 3, 6, 16, 20), or a counter (Claims 26-29), a transistor coupled across the capacitor (Claims 7, 21) or a current source (Claims 8, 23-24) or "driving the enable signal to the active state" Claim (10-13).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Seng et al. discloses a start-up circuit with self-timing for a crystal oscillator.

Liu et al. disclose a start-up circuit with a low power mode for a crystal oscillator.

Noble discloses a start-up circuit with a quick start up.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph Chang
Patent Examiner
Art Unit 2817

JC